Engineering 90 Proposal
High Speed Time Domain Reflectometer for Structural Integrity Monitoring Applications

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Abstract

The development and construction of a high speed Time Domain Reflectometer (TDR) instrument is proposed. The instrument is intended for structural integrity monitoring applications in which discontinuities spaced on the order of 20 cm apart must be discerned. A modular data acquisition platform will allow flexibility in the choice of a host control interface, allowing the instrumentation to be embedded in various on-site target applications. Total development and implementation expenditures are estimated to not exceed $500, excluding the cost of preexisting equipment and development systems.

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1 Introduction

Time domain reflectometry technology finds application in cable and transmission line characterization, in geotechnology for determining groundwater table levels and soil properties, and also in the oil industry for locating underground reserves. The proposed 20 cm resolution renders the instrument suitable for use in the monitoring of the structural integrity of dams and other large concrete structures in which a test cable can be embedded. Thus changes in the cable dielectric due to structural stresses or water seepage can be observed with the TDR instrumentation, and the location of the discontinuities can also be discerned.

Due to the very fast propagation of electromagnetic energy in wires, high bandwidth circuitry must designed to accurately characterize the cable under test. Parasitic elements in active device packaging and circuit board construction normally neglected in low frequency design may significantly affect the operation of the device.

This document details the technical underpinnings of the proposed instrument and provides an outline for the development process. Performance specifications for the final product will be presented, as well as a consideration of the feasibility of the project within the constraints of the manufacturing and measurement instrumentation capabilities available to the Engineering Department at Swarthmore College.

2 Technical Discussion

2.1 Operating Principle

The operating principle of time domain reflectometry is that an ideal square pulse of energy is transferred to the device under test (DUT), and the electromagnetic reflection of the energy is measured as a function of time. For the cable characterization, the transmission energy is an ideally square wave voltage. Reflection of the transmitted energy is observable as changes in the voltage on the cable at the point of injection, and by measuring this voltage as a function of time, the nature of the cable can be observed. Variation in the cable dielectric material and the distance of the discontinuities from the point of injection can be readily determined given the propagation velocity along the cable.

2.2 Device Structure

The general path of execution for acquiring one data point is now outlined. A block diagram of the acquisition engine is provided in Figure 1 for reference.

To acquire one data point, the microcontroller (ADuC7026) configures the time base to 1) start the step generator and 2) initiate the sample/hold circuit after a precise time delay. Once the sample/hold has been triggered and the sampled voltage stabilizes, the voltage is read by the A/D converter, stored in memory, and the process repeats with a different time delay for the next data point in the waveform. It is assumed that by the time the next data point is acquired, energy reflections in the cable have dissipated to a negligible level. Since each time delay value effectively corresponds to a single point along the wire, a complete characterization of the wire as a function of distance can be determined by incrementing the time delay by an appropriate amount. This methodology is an equivalent-time sampling, since the data points are acquired one by one to create the waveform instead of by a very fast continuously running sampler. The proposed instrument is

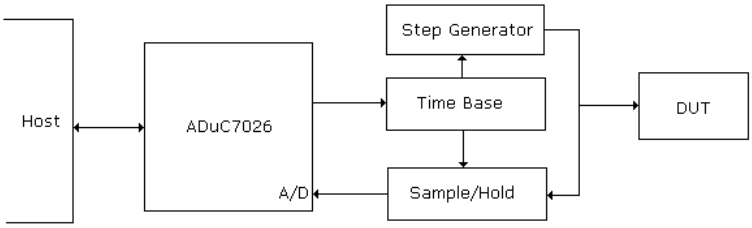

Figure 1: Block Diagram of TDR Data Acquisition System

for single-ended operation with 50 Ω SMA type cables. If time permits, a differential-mode version may be explored.

2.3 Performance Specification

Preliminary requirements can be arrived at through consideration of the desired device resolution and speed.

2.3.1 Step Generator Requirement

The central determining factor in designing the step generator is the speed of energy propagation in the test medium. The propagation velocity is determined by the dielectric material that separates the conductors in the cable, quantified by the relative dielectric constant. The relative dielectric constant can be related to the velocity of propagation as indicated below.

$$\epsilon_R = \frac{\epsilon_S}{\epsilon_0} = \frac{1}{v^2 \mu_0 \epsilon_0}$$

The roundtrip time for a pulse over a length l is given by

$$t_{RT} = \frac{2l}{v}.$$

Typical dielectric constants for various cables generally range between 2 and 4. The propagation velocities for these two values are calculated below, as well as the 20 cm roundtrip travel time.

$$\epsilon_R = 2 = \frac{1}{v^2(4\pi \cdot 10^{-7})(8.85 \cdot 10^{-12})},\ v = 2.12 \cdot 10^8 \text{ m/s}$$

$$\epsilon_R = 4 = \frac{1}{v^2(4\pi \cdot 10^{-7})(8.85 \cdot 10^{-12})},\ v = 1.49 \cdot 10^8 \text{ m/s}$$

$$t_{RT} = \frac{2 \cdot 0.2}{2.12 \cdot 10^8} = 1.8 \text{ ns}$$

$$t_{RT} = \frac{2 \cdot 0.2}{1.49 \cdot 10^8} = 2.6 \text{ ns}$$

If the minimum rise time for the step generator is taken as equal to the roundtrip travel time, then it seems that rise times on the order of 2 ns are required to resolve cable discontinuities spaced approximately 20 cm apart. To ensure the accuracy of the acquired data, rise times in the range of 1 ns will be considered as the preliminary specification for the step generator.

2.3.2 Sample/Hold Bandwidth Requirement

It is now assumed that the sample/hold amplifier circuit can be modeled to have a dominant pole response with the transfer function

$$A(s) = \frac{K}{s + \omega_0}.$$

The step response of this transfer function is illustrated below in Figure 2.

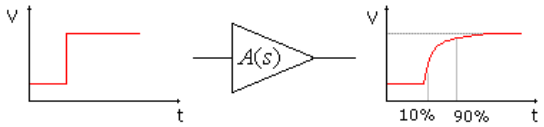

Figure 2: Step Response of SHA

After one time constant, the output voltage is at approximately 62% of the final value, and a upper bound estimate for the time required to go from 10% to 90% can be approximated as two time constants, 2τ. For a rise time of 1 ns, τ and the 3dB frequency are calculated below.

$$1ns = 2\tau$$
$$\tau = RC = 0.5 \cdot 10^{-9} \text{ s}$$
$$\omega_0 = \frac{1}{RC} = \frac{1}{\tau} = 20 \cdot 10^8$$
$$f = \frac{\omega}{2\pi} = 318 \text{ MHz}$$

For rise time of 1 ns, the frequency bandwidth is 318 MHz. It should be noted that due to the equivalent time sampling methodology, the sampling rate does not have to be very high. Rather the sampler must be designed to track a rapidly changing voltage and latch the voltage value very quickly.

2.3.3 Repetition Rate

It is assumed that the maximum number of data points per waveform is 2048. If four waveforms are to be acquired per second, each data point must be acquired in less than 122 μs. A rough time estimate is given for the acquisition of one data point.

Setup D/A Converter, Counter	30 μS
Step Generation	1 ns
Sampling Delay	(variable but relatively small)
Sample/Hold Setup Time	1 μS
A/D Conversion	1 μS
A/D Read	1 μS
Data Transfer	30 μS
Total	60-70 μS per data point.

Thus the waveform throughput performance goal should not prove difficult to achieve.

2.4 Component Overview

An overview of the various components in the TDR block diagram is now pursued.

2.4.1 Host Controller

The host is the device that controls the acquisition engine. It may set high level parameters such as the start time, number of data points per waveform, and the spacing between adjacent data points. The host then requests the microcontroller to perform the acquisition, and waits until it is completed. The acquired waveform is then transferred from the microcontroller memory to the host. The host may also interrupt an acquisition in progress to cancel or restart it. A clearly defined communication protocol will be developed to enable flexibility in the choice of the host device. Currently a 16 bit general input/output interface is being considered. Other options worthy of consideration are a Serial Peripheral Interface (SPI), or a standard RS-232 serial link. Using a standardized serial or generic parallel hardware interface allows the acquisition hardware to be interfaced directly with a variety of host devices, including a PC or an embedded system, in a straightforward manner.

2.4.2 Acquisition Microcontroller

The ADuC7026 is a 32-bit ARM microcontroller designed by Analog Devices specifically for data acquisition engines. It provides 4 built-in 12-bit D/A converters, a 12 channel 1MS/s 12-bit A/D converter, 8k SRAM, 62k FLASH, as well as support for UART (RS-232) serial and SPI communications. The device has a large number of general purpose I/O pins suitable for configuring and controlling the time base and for interfacing with the host. The GCC-ARM7 C compiler is readily available for developing the microcontroller code.

2.4.3 Time Base

The time base consists of a precision D/A converter, oscillator, counter, one-shot trigger, ramp generator, and comparator. A conceptual diagram of the time base is given in Figure 3.

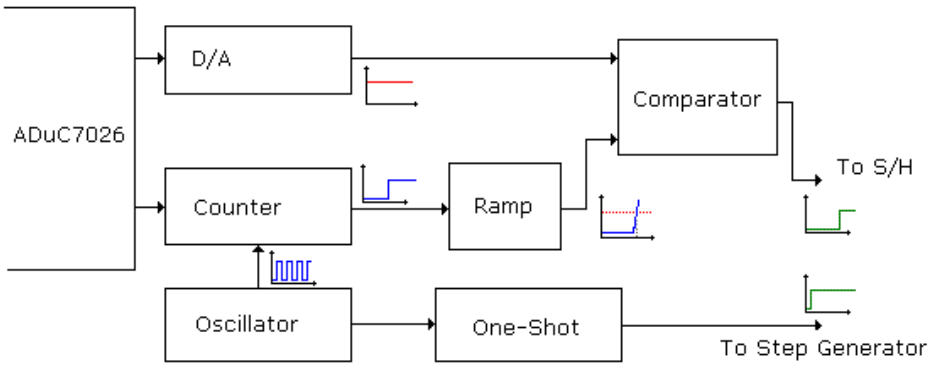

Figure 3: Time Base Structure

The microcontroller first configures the count value in the down-counter, and sets a voltage level with the D/A converter. Once the time base has been configured, the oscillator is enabled, which immediately triggers the one-shot device and thus the step generator. The counter decrements until it reaches 0, at which point the ramp circuit is started. When the voltage of the ramp exceeds the level set by the D/A converter, the comparator output flips, thereby triggering the sample/hold circuit to sample the voltage on the DUT. This two-part delay strategy allows for very fine adjustment of the sampling delay over a large range without requiring extremely high clock speeds.

2.4.4 Step Generator

The step generator propagates a voltage step in the cable. Due to the high switching speed required for precise resolution in the acquired waveform, packaged common-mode logic (CML) integrated circuits will probably be required for the desired performance. A possible implementation could be based on the Maxim MAX3841 2x2 crosspoint switch IC, which has 12 Gbps switching capability, and can provide rise times (10% to 90%) on the order of 30-60 pS. Potential discrete designs are also being pursued.

2.4.5 Sample and Hold

The high bandwidth sampler will most likely prove to be the most complex part of the acquisition system. The design will be based on differential bipolar topologies, potentially based on medium scale integrated (MSI) circuits for close matching and superior performance. Research into various circuit topologies capable of meeting performance demands is currently being pursued. Currently a bipolar diode bridge sampling switch circuit seems most promising.

2.5 Basic Calibration

Basic device calibration will performed in software. A known length of test cable can be placed between the step generator/sampler and the test connector. If nothing is connected, calibration constants for the step amplitude and time base can be determined by performing an unterminated acquisition and analyzing the resulting waveform.

2.6 Constraints

2.6.1 Construction Considerations

Due to the high frequency operation of the data acquisition circuit, special care must be taken with PCB layout. Surface mount components will be required, and low cost fabrication methods could involve using a laser-cut stencil with solder paste to accurately align the fine pitch SMT pads.

2.6.2 Instrumentation Limitations

Measurement instrumentation limitations may also prove to be an obstacle. The Engineering Department has a Tektronix 11801C Digital Sampling Oscilloscope that should be capable of readily measuring all of the signals in the circuit.

3 Project Plan Overview

3.1 Timeline and Milestones

At the writing of this document, the ADuC7026 microcontroller development kit has been obtained and tested. Research into high bandwidth samplers is currently underway, and a textbook on the subject should arrive in the next week. There are two primary milestones for the project: 1) a preliminary schematic and layout by the last week of January 2006, and 2) a workable prototype acquisition board with host communication facilities by the first week of March 2006.

3.2 Qualifications

The TDR instrument project in question is an appropriate choice for the designer due to its focus on high frequency analog circuitry and embedded systems development. The proposals author has in recent work focused on discrete analog designs, and has in the past worked on several embedded systems programming projects.

3.3 Cost Analysis

Many of the major items required for developing the TDR instrument have already been purchased for previous experimentation and are thus not included in this cost estimate. Development kits for the ADuC7026 and MAX3841 are already available to the designer. Simulation and PCB layout software is owned by the Engineering Department. As a result, the costs remaining involve PCB manufacturing, stencil manufacturing, and parts. The total cost of components for a prototype acquisition board should not exceed $100, as the ADuC7026 and MAX3841 are priced approximately $25 and $11 each, respectively. The ADuC7026 is available from DigiKey, and the MAX3841 directly from Maxim Inc. Availability is not a critical concern, as the development kits have already been obtained. Since the project calls for building a prototype TDR instrument, these parts will still need to be ordered reasonably soon, even though not having them will not delay product development. The remaining surface mount active and passive components should not sum to a significant total. The manufacturing cost of one double sided 11x5 PCB with single-sided silkscreen from Advanced Circuits included UPS Ground shipping is approximately $49. The price of a laser-cut stencil from Advanced Circuits is approximately $150. As a result, the upper bound of project costs is placed at a reasonable $500.

4 Critical Path Method

A Critical Path Method (CPM) analysis is presented. A detailed task list is indicated in Table 1. The network diagram with earliest and latest task start times is shown in Figure 4. The Gantt Chart follows in Figure 5. The total duration from start to finish is estimated at 72 days, which seems reasonable for a 14 week (98 day) semester.

Table 1: Critical Path Method Task List

Task	Description	Duration	Needs	Feeds
A	Determine preliminary specifications	1d	-	B
B	Perform calculations to determine performance requirements	1d	A	C
C	Research potential circuit topologies to implement block diagram	2wk	B	D
D	Design circuits, simulate with SPICE	1wk	C	G
E	Design host/device communication protocol and hardware interface	2d	-	F
F	Implement host/device communication software/hardware	1wk	E	I,G
G	Design prototype PCB with careful layout consideration	3d	D,F	H
H	Order necessary SMT parts, PCB, and solder stencil	2wk	G	I
I	Perform testing of circuit board	1wk	F,H	J
J	Make revisions to circuit, build revised prototype	3wk	I	K
K	Prepare and assemble documentation	4wk	-	L
L	Write final report	4d	K,J	-

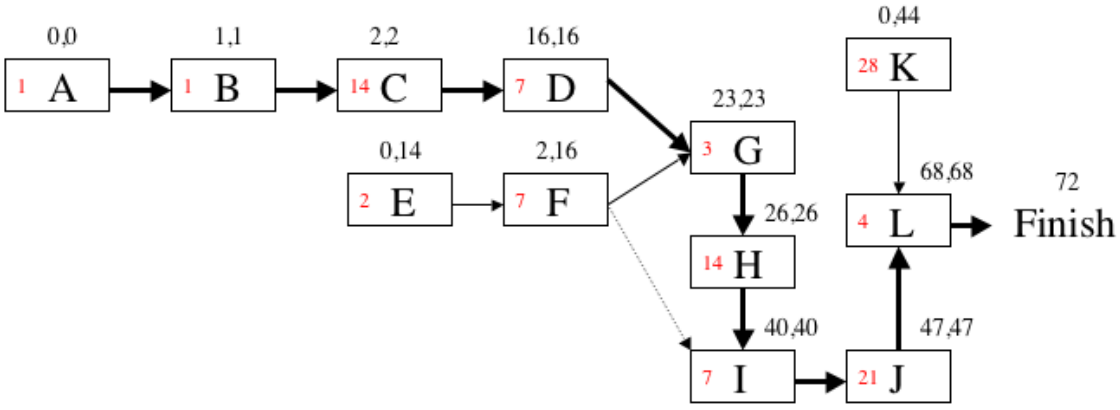

Figure 4: Critical Path Method Network Diagram

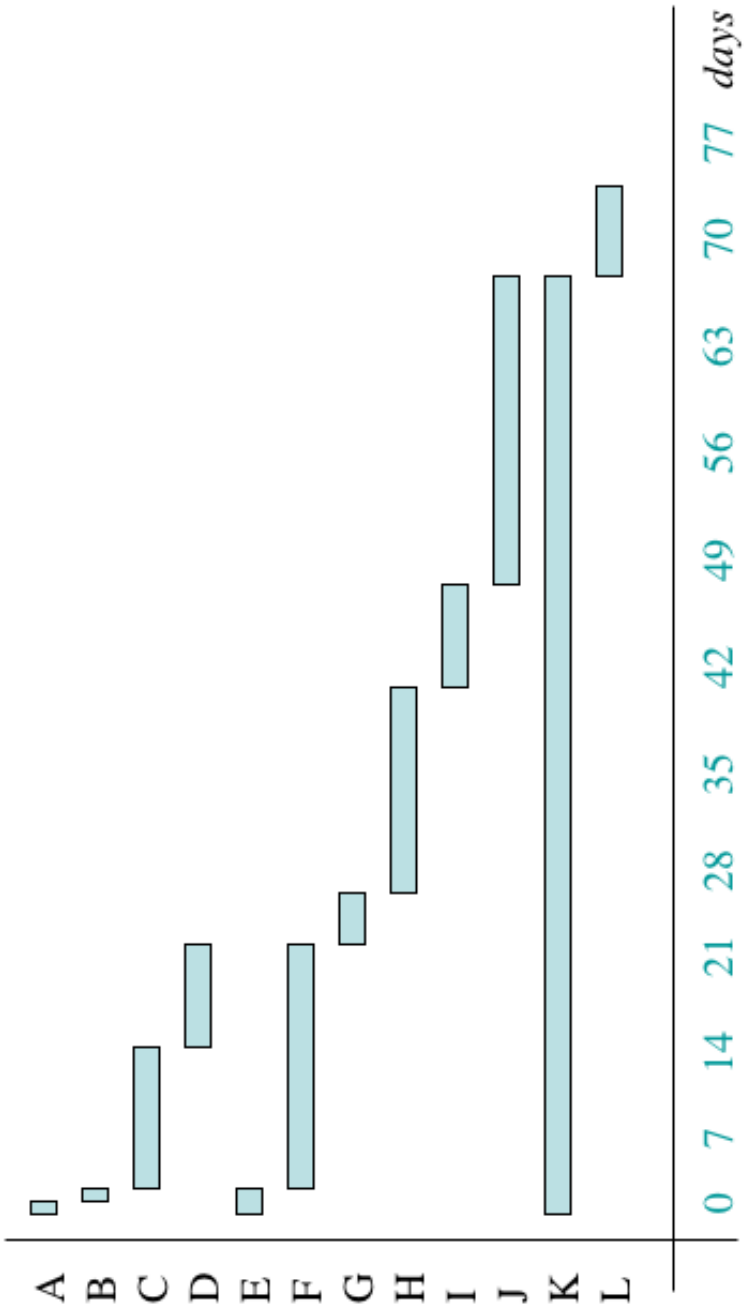

Figure 5: Critical Path Method Gantt Chart

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